



A 2DLNS based Multiplier and Accumulator (MAC) unit

Mahzad Azarmehr

Supervisor: Dr. R. Muscedere

University of Windsor

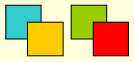
Electrical and Computer Engineering

Summer 2006



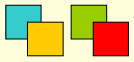
Outline

- Multidimensional Logarithmic Number System
 - Introduction
 - Representation
 - Properties
 - Calculations
 - Conversion
- Multiplier and Accumulator unit
 - Definition
 - Design Specifications
 - RTL Organization
 - Synthesis



Introduction

- **Desired characteristics of a number system used in DSP:**
 - More error-free mapping approximations
 - Less complexity of arithmetic operations
 - Smaller size of corresponding representations
 - More accurate representation of smaller values



MDLNS (Representation)

- A representation of the real number X , in the form:

$$x = \sum_{i=1}^n s_i \prod_{j=1}^b p_j^{e_j^{(i)}}$$

- where s_i is sign, p_j can be real, and $e_j^{(i)}$ are integers, is called an n digit multi-dimensional logarithmic representation of X
- b is the number of bases used (at least two) and the first one, p_1 will always be assumed to be 2



MDLNS (Properties)

- A large reduction in hardware
- An attendant reduction in complexity of the hardware
- Ability to choose the best possible representation for each application



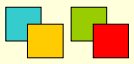
MDLNS (Calculations)

- **Multiplication and Division**

Given a single-digit representation of $x=\{s_x, a_x, b_x\}$ and $y=\{s_y, a_y, b_y\}$:

$$x.y = \{ s_x \text{ xor } s_y, a_x + a_y, b_x + b_y \}$$

$$x \div y = \{ s_x \text{ xor } s_y, a_x - a_y, b_x - b_y \}$$



MDLNS (Calculations)

- **Addition and Subtraction**

$$2^{a_x} \cdot D^{b_x} + 2^{a_y} \cdot D^{b_y} = (2^{a_x} \cdot D^{b_x}) \cdot (1 + 2^{a_y - a_x} \cdot D^{b_y - b_x})$$
$$\approx (2^{a_x} \cdot D^{b_x}) \cdot \Phi(a_y - a_x, b_y - b_x)$$

$$2^{a_x} \cdot D^{b_x} - 2^{a_y} \cdot D^{b_y} = (2^{a_x} \cdot D^{b_x}) \cdot (1 - 2^{a_y - a_x} \cdot D^{b_y - b_x})$$
$$\approx (2^{a_x} \cdot D^{b_x}) \cdot \Psi(a_y - a_x, b_y - b_x)$$

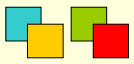
The operators Φ and Ψ are lookup tables that store the precomputed 2DLNS values.



MDLNS (Conversions)

$$x = \sum_{i=1}^n s_i \cdot 2^{a_i} \cdot D^{b_i}$$

- If R bits are considered to represent second base (D) exponent, $b_i = \{-2^{R-1}, \dots, 2^{R-1}\}$ and range of a_i is determined regarding to D and Q digit equivalent binary data
- b is used as an index address to a LUT to find a pseudo-floating point representation for D^b and finally a normalized binary expression for the 2DLNS representation



MDLNS (Conversions)

- The pseudo-floating point representation is in the form $\mu(b) \cdot 2^{\varepsilon(b)}$, where $\mu(b)$ is the mantissa (real) and $\varepsilon(b)$ is the exponent (integer).

$$x = s \cdot \mu(b) \cdot 2^{(a + \varepsilon(b))}$$

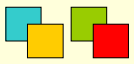
- To convert a binary representation to a single-digit 2DLNS, the normalized mantissa, $\mu(b)$, would be the input to the LUT.



Conversion Look-up Table

- Conversion LUT for $D = 3$, $R = 3$, $C = 10$

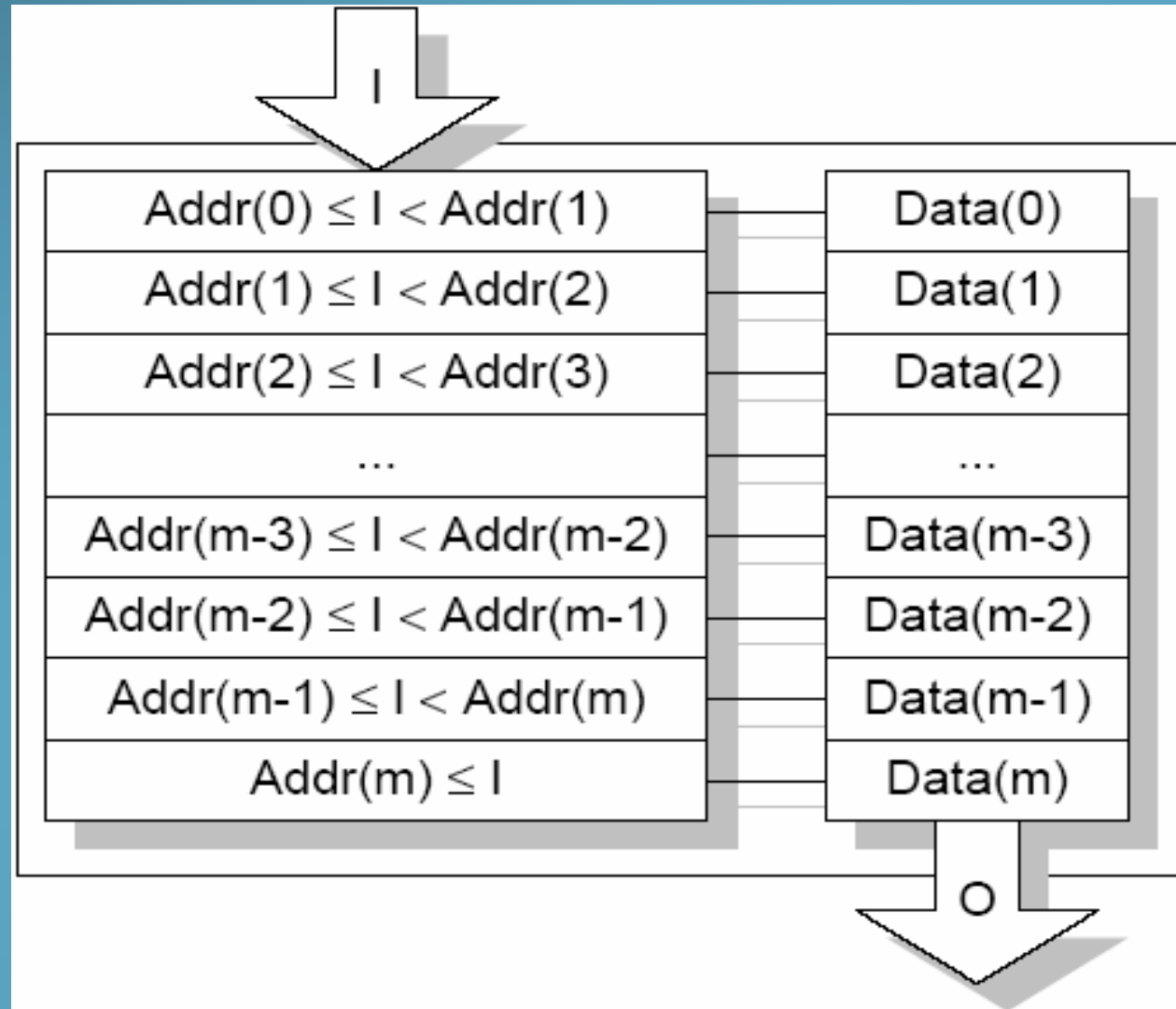
Input	Output	
$\mu(D^b)$ (base 2)	$\varepsilon(D^b)$	b
1.0000000000	0	0
↓	?	?
1.0010000000	3	2
↓	?	?
1.0010111101	-5	-3
↓	?	?
1.0101010101	-2	-1
↓	?	?
1.1000000000	1	1
↓	?	?
1.1001010010	-7	-4
↓	?	?
1.1011000000	4	3
↓	?	?
1.1100011100	-4	-2
↓	?	?



Range Addressable Look-Up Table (RALUT)

- Size of LUT can be reduced by a decrease in number of rows from 2^C (which C is the number of decimal point digits of mantissa) to $2^R + 1$
- A RALUT differs from the classic LUT by changing the address decoder system to match on a range of values rather than exact values

RALUT Structure





Range Addressable Look-Up Table (RALUT)

- Most of the designs which are used in MDLNS circuits can be efficiently implemented with RALUTs.
- The proper second base (optimal base) should be selected in accordance to the specific design consideration.
- Size of RALUTs and their contents should be adjusted based on optimal bases and necessary precisions.



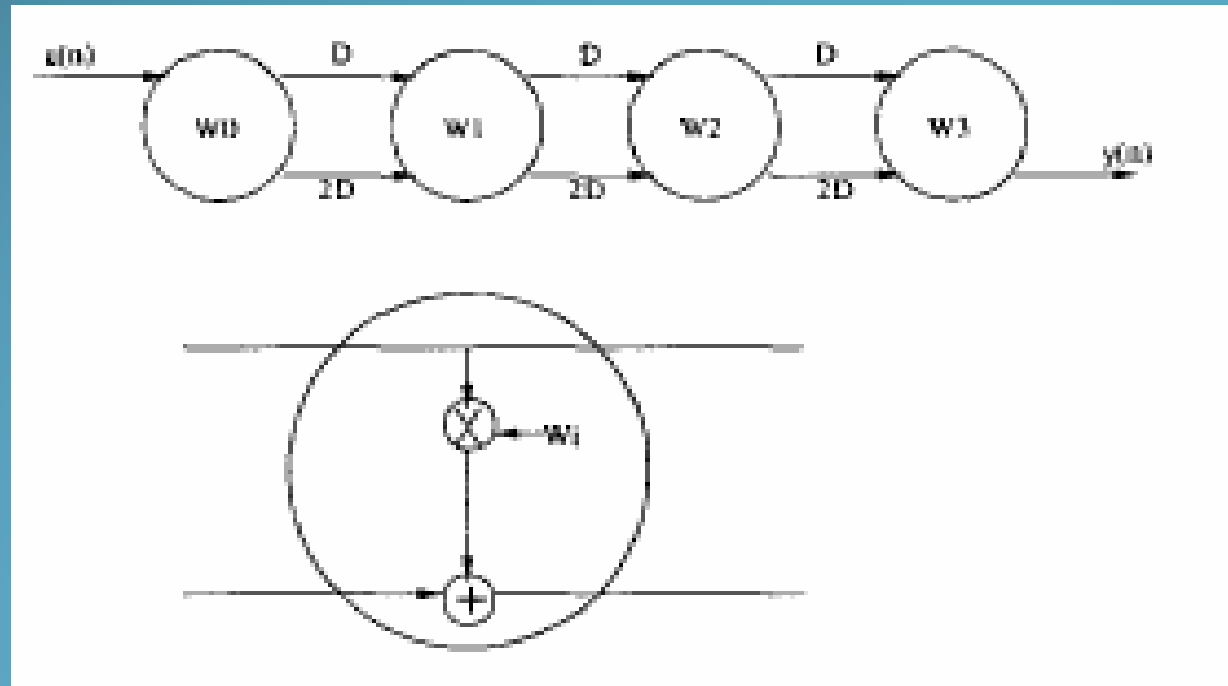
Multiplier and Accumulator (MAC) unit

- A MAC multiplies corresponding elements of two sequences of numbers $\{X_i\}$ and $\{Y_i\}$ and accumulates the sum of the products:

$$P = \sum_i X_i \cdot Y_i$$

- The implementation of a MAC needs intensive computation and consumes much resources. There is always a traditional trade off of size versus speed.

MAC in FIR filter

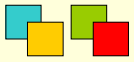


$$y[n+1] = y[n] + x(n) \cdot w(n)$$

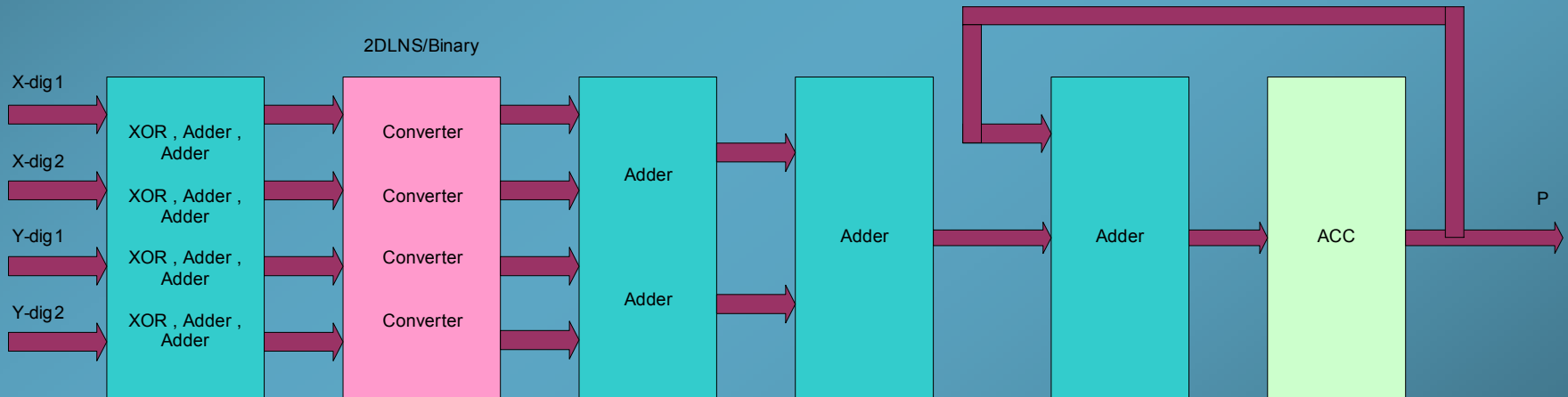


MAC unit (Specifications)

- Coefficients :
2-digit 2DLNS numbers ($D = 1.28308348549366$, $B = 6$, $R = 3$)
- Input data :
2-digit 2DLNS numbers ($D = 1.28308348549366$, $B = 6$, $R = 5$)
- There are four partial products for each pair of numbers.
- Multiplications are performed in 2DLNS, but partial products are converted to Binary to be added.



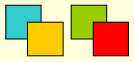
MAC unit (Structure)



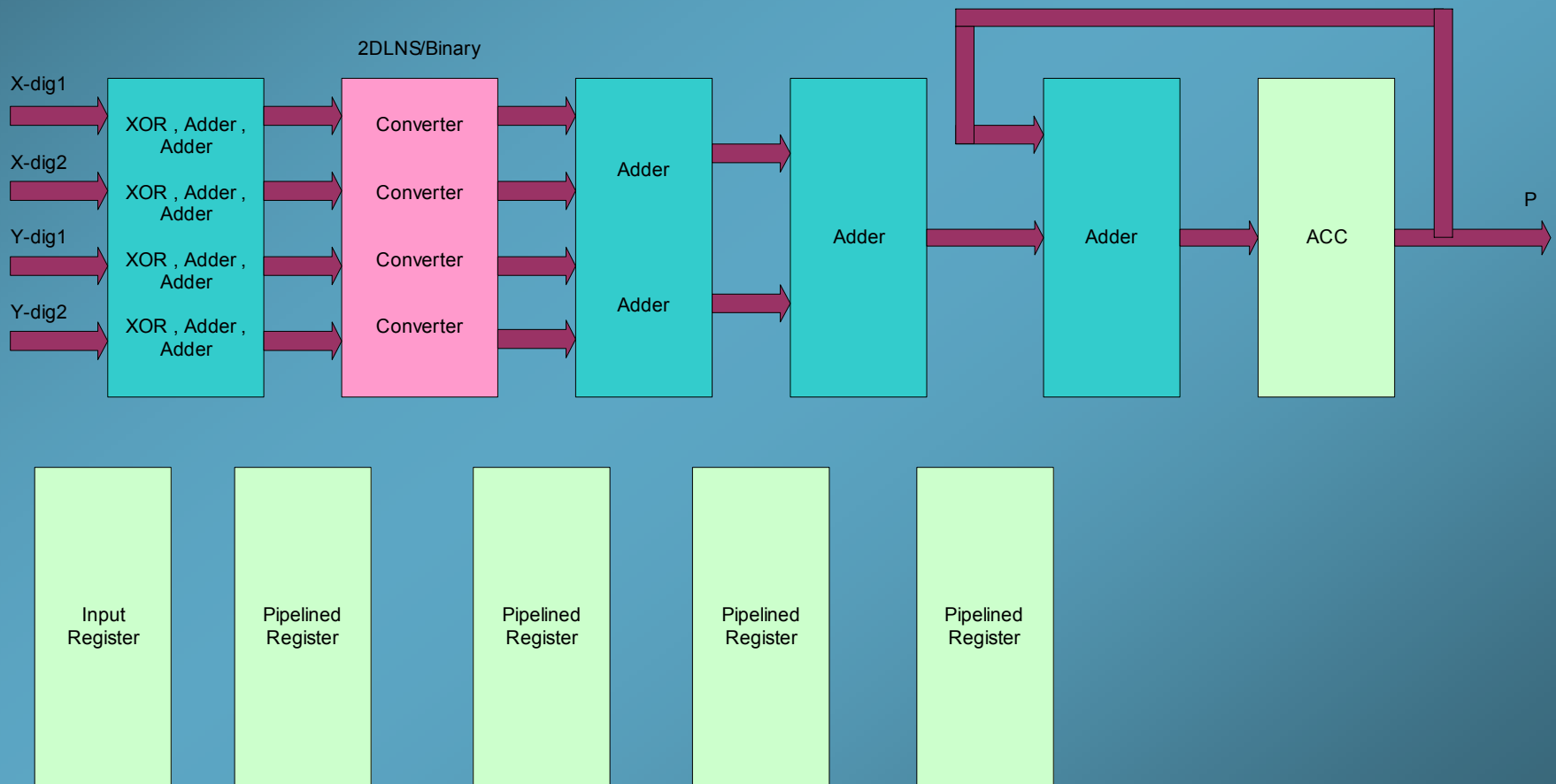


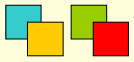
MAC unit (Pipelined)

- The time taken to complete processing one pair of inputs is the sum of the delays for all stages. This delay can be avoided by pipelining the MAC.
- The advantage of pipelined approach is that the clock period can be reduced to the slowest of the pipeline stages, rather than the total of their delays.
- The more efficiency for pipelining is the case that each stage performed in just one clock cycle.



MAC unit (Pipelined Structure)



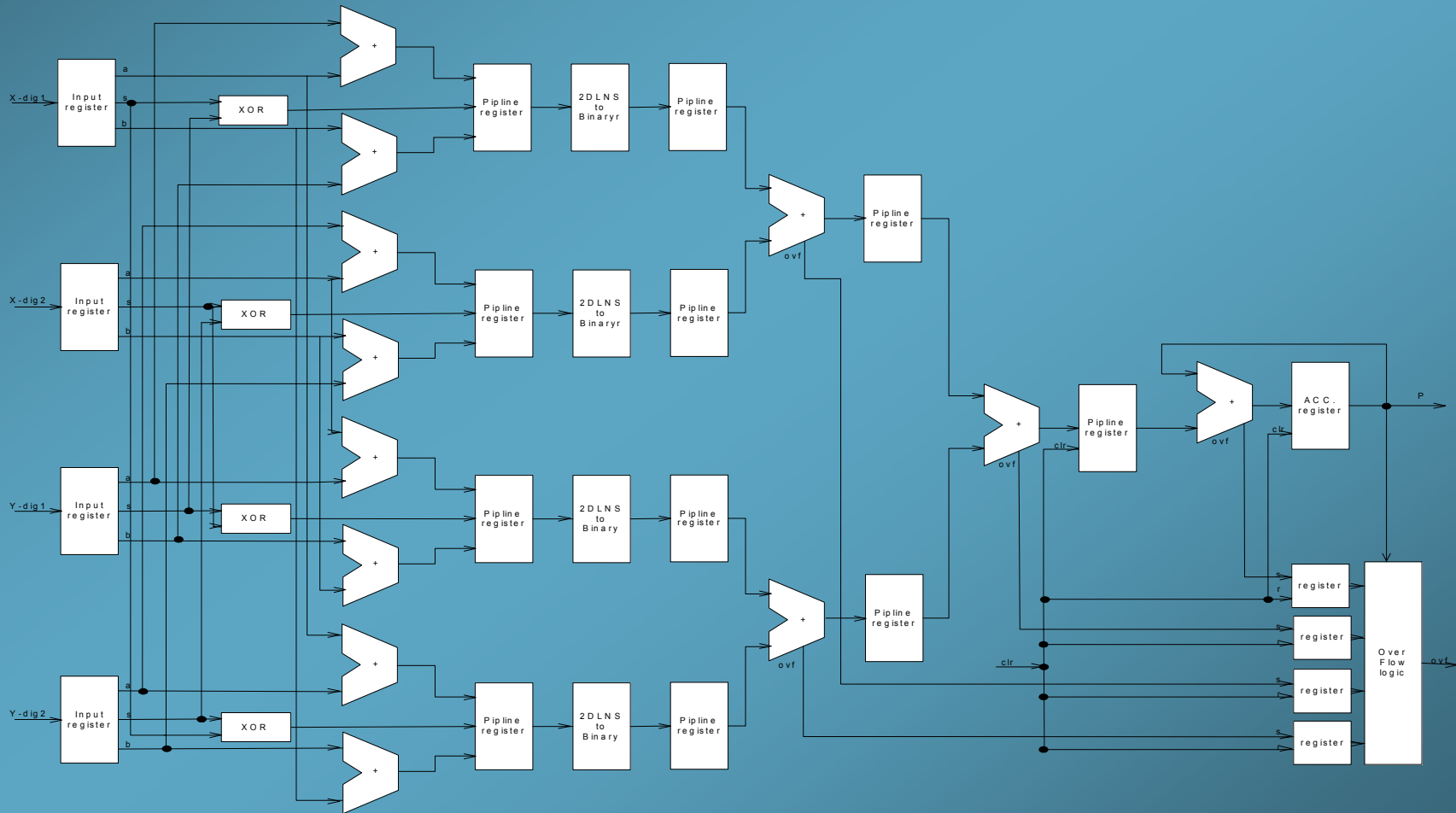


MAC unit (Overflow)

- Overflow in intermediate partial sums; an overflow flag must be set
- Overflow in the final accumulation (may be a transient condition);
 - Expansion the range used to represent result
 - An overflow flag must be set
- The final overflow signal is an OR combination of all overflow flags



MAC unit (RTL organization)





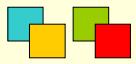
MAC unit (Reduced RALUT)

- Second base exponent (B) of Input data can be limited in range -12 to 12 instead of -16 to 15. Since intermediate sums can be shown by $R = 5$ instead of $R = 6$, a RALUT with almost half size can be used.
- This means to force data from order of 2^{-40} be limited to order of 2^{-37} .
- However, all possible representations should be checked beforehand in terms of acceptable mapping precision.



MAC unit (Synthesis Results)

<i>Factor</i>	R = 6 Clock-pulse = 10(ns)	R = 5 Clock-pulse = 8(ns)
<i>Data required time (ns)</i>	9.35	7.85
<i>Data arrival time (ns)</i>	-9.35	-7.85
<i>Slack (ns)</i>	0.00	0.00
<i>Total cell Area (μm^2)</i>	284496.5625	119642.1094
<i>Total Dynamic Power (mw)</i>	10.9670	9.8602



A 2DLNS based Multiplier and Accumulator (MAC) unit

Questions and Comments